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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/824,988	Applicant(s) HUGHES ET AL.	
	Examiner Aimee J Li	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2001 and 10 April 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4, 5, and 6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-49 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Request to rescind non-publication request as filed on 25 September 2001; Pre-amendment A as filed 25 July 2001; IDS as filed 23 July 2001; IDS as filed 13 November 2002; and IDS as filed 10 March 2003.

Priority

3. Acknowledgement is made of application's claim of priority to Provisional Application Serial Number 60/224,368 filed August 9, 2000.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4, 11-24, 31-36, and 43-49 are rejected under 35 U.S.C. 102(b) as being taught by James L. Turley's Advanced 80836 Programming Techniques (herein referred to as Turley).

7. Referring to claim 1, Turley has taught an apparatus comprising:

a. A first storage location configured to store a first indication, the first storage location addressable by a first instruction defined by a processor architecture (Turley pages 18-34, 47-54, 79-81, 142-145, and 178);

b. A second storage location configured to store a second indication, the second storage location addressable by a second instruction defined by the processor architecture, the second instruction being different from the first instruction (Turley pages 18-34, 47-54, 79-81, 142-145, and 178);

c. A third storage location configured to store a mode indication, the mode indication indicative of whether or not a first mode defined in the processor architecture is active (Turley pages 18-34, 47-54, 79-81, 142-145, and 178); and

d. A processor configured to generate the mode indication responsive to the first indication and the second indication (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

8. Referring to claim 2, Turley has taught wherein the first indication is an enable indication defined in the processor architecture to indicate whether or not the first mode is to be enabled (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

9. Referring to claim 3, Turley has taught wherein the second indication is a paging indication defined in the processor architecture to indicate of whether or not paging is enabled (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

10. Referring to claim 4, Turley has taught wherein the mode indication indicates that the first mode is active if the enable indication is in an enabled state and the paging indication indicates that paging is enabled (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

11. Referring to claim 11, Turley has taught a fourth storage location configured to store a segment selector identifying a segment descriptor including a first operating mode indication and a second operating mode indication (Turley pages 18-34, 47-54, 79-81, 142-145, and 178), and wherein the processor is configured to generate an operating mode responsive to the mode indication, the first operating mode indication, and the second operating mode indication (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

12. Referring to claim 12, Turley has taught wherein the first storage location is located within a first register defined by the processor architecture, and wherein the second storage location is located within a second register defined by the processor architecture (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

13. Referring to claim 13, Turley has taught wherein the third storage location is located within the first register (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

14. Referring to claim 14, Turley has taught wherein the first register and the second register are incorporated within the processor (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

15. Referring to claim 15, Turley has taught a circuit coupled to the first register and the second register, wherein the circuit is configured to generate the mode indication for storage in the third storage location (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

16. Referring to claim 16, Turley has taught wherein the processor implements the processor architecture (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

17. Referring to claim 17, Turley has taught wherein the processor emulates the processor architecture (Turley pages 27 and 259-260).

18. Referring to claim 18, Turley has taught wherein the processor executes interpreter software for interpreting instructions defined in the processor architecture (Turley page 27 and 259-260).

19. Referring to claim 19, Turley has taught wherein the processor executes translator software for translating instructions defined in the processor architecture to instructions executable by the processor (Turley page 27 and 259-260).

20. Referring to claim 20, Turley has taught wherein the processor executes a combination of: (i) interpreter software for interpreting instructions defined in the processor architecture (Turley page 27 and 259-260); and (ii) translator software for translating instructions defined in the processor architecture to instructions executable by the processor (Turley page 27 and 259-260).

21. Referring to claim 21, Turley has taught a processor comprising:

a. A first register configured to store a first indication, the first register addressable by a first instruction (Turley pages 18-34, 47-54, 79-81, 142-145, and 178);

b. A second register configured to store a second indication, the second register addressable by a second instruction different from the first instruction (Turley pages 18-34, 47-54, 79-81, 142-145, and 178); and

c. A circuit coupled to the first register and the second register, wherein the circuit is configured to generate a mode indication responsive to the first indication and the second indication (Turley pages 18-34, 47-54, 79-81, 142-145, and 178),

d. Wherein the mode indication is indicative of whether or not a first mode defined in a processor architecture of the processor is active (Turley pages 18-34, 47-54, 79-81, 142-145, and 178), and

e. Wherein the circuit is configured to store the mode indication in a location addressable by an instruction (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

22. Referring to claim 22, Turley has taught wherein the first indication is an enable indication defined in the processor architecture to indicate whether or not the first mode is to be enabled (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

23. Referring to claim 23, Turley has taught wherein the second indication is a paging indication defined in the processor architecture to indicate of whether or not paging is enabled (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

24. Referring to claim 24, Turley has taught wherein the mode indication indicates that the first mode is active if the enable indication is in an enabled state and the paging indication indicates that paging is enabled (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

25. Referring to claim 31, Turley has taught a segment register configured to store a segment selector identifying a segment descriptor including a first operating mode indication and a second operating mode indication (Turley pages 18-34, 47-54, 79-81, 142-145, and 178), and wherein the circuit is configured to generate an operating mode responsive to the mode indication, the first operating mode indication, and the second operating mode indication (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

26. Referring to claim 32, Turley has taught wherein the mode indication is also stored in the first register (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

27. Referring to claim 33, Turley has taught a method comprising:

a. Storing a first indication in a first storage location addressable by a first instruction (Turley pages 18-34, 47-54, 79-81, 142-145, and 178);

b. Storing a second indication in a second storage location addressable by a second instruction (Turley pages 18-34, 47-54, 79-81, 142-145, and 178);

c. Generating a mode indication indicative of whether or not a first mode defined in a processor architecture is active, the generating responsive to the first indication and the second indication (Turley pages 18-34, 47-54, 79-81, 142-145, and 178); and

d. Storing the mode indication in a third addressable storage location (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

28. Referring to claim 34, Turley has taught wherein the first indication is an enable indication defined in the processor architecture to indicate whether or not the first mode is to be enabled (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

29. Referring to claim 35, Turley has taught wherein the second indication is a paging indication defined in the processor architecture to indicate of whether or not paging is enabled (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

30. Referring to claim 36, Turley has taught wherein the generating comprises generating the mode indication to indicate that the first mode is active if the enable indication is in an enabled

state and the paging indication indicates that paging is enabled (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

31. Referring to claim 43, Turley has taught generating an operating mode responsive to the mode indication, a first operating mode indication, and a second operating mode indication (Turley pages 18-34, 47-54, 79-81, 142-145, and 178), wherein the first operating mode indication and the second operating mode indication are included in a segment descriptor identified by a segment selector stored in a fourth storage location (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

32. Referring to claim 44, Turley has taught a carrier medium carrying a set of instructions for activating a first mode in a processor, the set of instructions including:

a. A first one or more instructions to update a first indication to indicate that physical address extension is enabled (Turley pages 18-34, 47-54, 79-81, 142-145, and 178);

b. A second one or more instructions to update a page table base register to point to a set of page tables (Turley pages 18-34, 47-54, 79-81, 142-145, and 178);

c. A third one or more instructions to update an enable indication to an enabled state (Turley pages 18-34, 47-54, 79-81, 142-145, 163-168, and 178); and

d. A fourth one or more instructions to update a paging indication to indicate that paging is enabled (Turley pages 18-34, 47-54, 79-81, 142-145, 163-168, and 178);.

33. Referring to claim 45, Turley has taught wherein an order of the first one or more instructions, the second one or more instructions, and the third one or more instructions in the set of instructions is arbitrary (Turley pages 18-34, 47-54, 79-81, 142-145, 163-168, and 178).

34. Referring to claim 46, Turley has taught wherein the fourth one or more instructions are ordered subsequent to the first one or more instructions, the second one or more instructions, and the third one or more instructions in the set of instructions (Turley pages 18-34, 47-54, 79-81, 142-145, 163-168, and 178).

35. Referring to claim 47, Turley has taught wherein the set of instructions further includes a fifth one or more instructions to update the paging indication to indicate that paging is disabled, the fifth one or more instructions ordered prior to the first one or more instructions, the second one or more instructions, the third one or more instructions, and the fourth one or more instructions in the set of instructions (Turley pages 18-34, 47-54, 79-81, 142-145, 163-168, and 178).

36. Referring to claim 48, Turley has taught a carrier medium carrying a set of instructions for deactivating a first mode in a processor, the set of instructions including:

a. A first one or more instructions to update a paging indication to indicate that paging is disabled (Turley pages 18-34, 47-54, 79-81, 142-145, 163-168, and 178);

b. A second one or more instructions to update a page table base register to point to a set of page tables(Turley pages 18-34, 47-54, 79-81, 142-145, 163-168, and 178); and

c. A third one or more instructions to update an enable indication to a disabled state (Turley pages 18-34, 47-54, 79-81, 142-145, 163-168, and 178).

37. Referring to claim 49, Turley has taught wherein the set of instructions further includes a fourth one or more instructions to update the paging indication to indicate that paging is enabled (Turley pages 18-34, 47-54, 79-81, 142-145, 163-168, and 178).

Claim Rejections - 35 USC § 103

38. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

39. Claims 5-10, 25-30, and 37-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over James L. Turley's Advanced 80836 Programming Techniques (herein referred to as Turley), as applied to claims 3, 23, and 24 above, in view of Van Dyke et al., U.S. Patent Number 6,418,524 (herein referred to as Van Dyke).

40. Referring to claims 5-10 and 25-30, Turley has taught

a. Wherein the processor is configured to check a status of one or more indications including the enable indication when changing one of the one or more indications to ensure that the change is permitted by the processor architecture (Applicant's claims 5 and 25) (Turley pages 18-34, 47-54, 79-81, 142-145, and 178); and

b. Wherein the processor is configured to signal an exception prior to changing the one of the one or more indications if the change is not permitted (Applicant's claims 6 and 26) (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

41. Turley has not taught

a. Wherein the processor is configured to check a status of one or more indications including the paging indication (Applicant's claims 5 and 25);

b. Wherein, if the enable indication is changed from a disabled state to an enabled state, the processor checks that the paging indication indicates that paging is disabled for the change to be permitted (Applicant's claims 7 and 27);

c. Wherein, if the enable indication is changed from an enabled state to a disabled state, the processor checks that the paging indication indicates that paging is disabled for the change to be permitted (Applicant's claims 8 and 28);

d. Wherein, if the paging indication is changed from indicating that paging is disabled to indicating that paging is enabled, the change is not permitted if the enable indication is in an enabled state and another indication indicates that physical address extension is disabled (Applicant's claims 9 and 29); and

e. Wherein the one of the one or more indications is an indication of whether or not physical address extension is enabled, and wherein the change is not permitted if the enable indication is in an enabled state (Applicant's claims 10 and 30).

42. Van Dyke has taught

a. Wherein the processor is configured to check a status of one or more indications including the paging indication (Applicant's claims 5 and 25) (Van Dyke column 1, lines 23-25 and 41-64; column 2, lines 14-54; Figure 1; and Figure 2);

b. Wherein, if the enable indication is changed from a disabled state to an enabled state, the processor checks that the paging indication indicates that paging is

disabled for the change to be permitted (Applicant's claims 7 and 27) (Van Dyke column 1, lines 23-25 and 41-64; column 2, lines 14-54; Figure 1; and Figure 2);

c. Wherein, if the enable indication is changed from an enabled state to a disabled state, the processor checks that the paging indication indicates that paging is disabled for the change to be permitted (Applicant's claims 8 and 28) (Van Dyke column 1, lines 23-25 and 41-64; column 2, lines 14-54; Figure 1; and Figure 2);

d. Wherein, if the paging indication is changed from indicating that paging is disabled to indicating that paging is enabled, the change is not permitted if the enable indication is in an enabled state and another indication indicates that physical address extension is disabled (Applicant's claims 9 and 29) (Van Dyke column 1, lines 23-25 and 41-64; column 2, lines 14-54; Figure 1; and Figure 2); and

e. Wherein the one of the one or more indications is an indication of whether or not physical address extension is enabled, and wherein the change is not permitted if the enable indication is in an enabled state (Applicant's claims 10 and 30) (Van Dyke column 1, lines 23-25 and 41-64; column 2, lines 14-54; Figure 1; and Figure 2).

43. In regards to Van Dyke, teaching that segmentation and paging are dependent means that one must indicate the correct mode in order for the other to be enabled. A person of ordinary skill in the art at the time the invention was made, and as taught by Van Dyke, would have recognized that having segmentation and paging dependent allows compatibility and use in newer and/or more advance microprocessor architectures (Van Dyke column 1, lines 60-64),

thereby increasing compatibility and usability. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the segmentation and paging dependency to increase compatibility and usability.

44. Referring to claims 37-42, Turley has taught

a. Checking a status of one or more indications including the enable indication and when changing one of the one or more indications to ensure that the change is permitted by the processor architecture (Applicant's claim 37) (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

b. Signaling an exception prior to changing the one of the one or more indications if the change is not permitted (Applicant's claim 38) (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

45. Turley has not taught

a. Checking a status of one or more indications including the enable indication and the paging indication (Applicant's claim 37);

b. Wherein the checking comprises, if the enable indication is changed from a disabled state to an enabled state, checking that the paging indication indicates that paging is disabled for the change to be permitted (Applicant's claim 39);

c. Wherein the checking comprises, if the enable indication is changed from an enabled state to a disabled state, checking that the paging indication indicates that paging is disabled for the change to be permitted (Applicant's claim 40);

d. Wherein, if the paging indication is changed from indicating that paging is disabled to indicating that paging is enabled, the change is not permitted if the

enable indication is in an enabled state and another indication indicates that physical address extension is disabled (Applicant's claim 41); and

e. Wherein the one of the one or more indications is an indication of whether or not physical address extension is enabled, and wherein the change is not permitted if the enable indication is in an enabled state (Applicant's claim 42).

46. Van Dyke has taught

a. Checking a status of one or more indications including the enable indication and the paging indication (Applicant's claim 37) (Van Dyke column 1, lines 23-25 and 41-64; column 2, lines 14-54; Figure 1; and Figure 2);

b. Wherein the checking comprises, if the enable indication is changed from a disabled state to an enabled state, checking that the paging indication indicates that paging is disabled for the change to be permitted (Applicant's claim 39) (Van Dyke column 1, lines 23-25 and 41-64; column 2, lines 14-54; Figure 1; and Figure 2);

c. Wherein the checking comprises, if the enable indication is changed from an enabled state to a disabled state, checking that the paging indication indicates that paging is disabled for the change to be permitted (Applicant's claim 40) (Van Dyke column 1, lines 23-25 and 41-64; column 2, lines 14-54; Figure 1; and Figure 2);

d. Wherein, if the paging indication is changed from indicating that paging is disabled to indicating that paging is enabled, the change is not permitted if the enable indication is in an enabled state and another indication indicates that

physical address extension is disabled (Applicant's claim 41) (Van Dyke column 1, lines 23-25 and 41-64; column 2, lines 14-54; Figure 1; and Figure 2); and

e. Wherein the one of the one or more indications is an indication of whether or not physical address extension is enabled, and wherein the change is not permitted if the enable indication is in an enabled state (Applicant's claim 42) (Van Dyke column 1, lines 23-25 and 41-64; column 2, lines 14-54; Figure 1; and Figure 2).

47. In regards to Van Dyke, teaching that segmentation and paging are dependent means that one must indicate the correct mode in order for the other to be enabled. A person of ordinary skill in the art at the time the invention was made, and as taught by Van Dyke, would have recognized that having segmentation and paging dependent allows compatibility and use in newer and/or more advance microprocessor architectures (Van Dyke column 1, lines 60-64), thereby increasing compatibility and usability. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the segmentation and paging dependency to increase compatibility and usability.

Conclusion

48. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

49. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

50. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
June 28, 2004

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